Name (5 pts)_____

ECE2700 Exam 2. Spring 2013. 5 Pages. Open book, Open Notes. Internet may be used to access the online text only. Cheating will result in a score of 0 for this exam.

Part 1. Short Answer.

1. (3 pts) Under what circumstances would you use a VEM instead of a Karnaugh map?

    _____

    _____

2. (3 pts) Put the following design steps in order (number them 1-5)
    _____ understand or develop an algorithm.
    _____ simulate and test from bottom-up.
    _____ get the requirements.
    _____ subdivide and repeat.
    _____ understand the concept (i.e. what it does).

3. (2 pts) (true/false) In VHDL, the order of *concurrent* statements does not matter, but the order of *sequential* statements does matter.

4. (2 pts) (true/false) The architecture part of a VHDL module defines the interface (i.e. the inputs and outputs) of that module.

5. (2 pts) In the architecture part of a module, the concurrent statements come (before/after) the keyword **begin**. (circle one)

6. (2 pts) The statements inside a VHDL process are (concurrent/sequential). (circle one)

7. (2 pts) (true/false) For assignment statements in VHDL, we use **<=** to assign a value to a signal and **:=** to assign a value to a variable.

8. (2 pts) Show how to represent the number 49 in BCD. _____

9. (2 pts) How many bits were originally used for the American Standard Code for Information Interchange (ASCII)?

    _____

10. (2 pts) (true/false) A demultiplexer can also be used as a binary to one-hot decoder.

11. (2 pts) (true/false) For combinational logic circuits, the output depends not only on present inputs but past inputs as well.

12. (3 pts) What problem can occur if an input to a flip-flop changes at nearly the same time as the clock goes high?

    _____

    _____

13. (4 pts) The amount of time a flip-flop's input must be stable before the clock edge is known as the _____ and the time a flip-flop's input must be stable after the clock edge is known as the _____.

14. (2 pts) (true /false) A good way to make a clock enable is to add an AND gate to the clock signal as shown below:
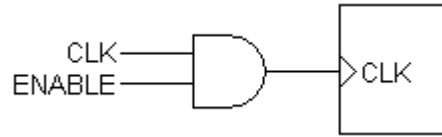
15. (3 pts) Explain the difference between a behavioral and a structural model.

_____

_____

_____

Part 2. Problems.

16. (8 pts) Loop and give the simplest SOP (sum of products) expression for each of the following Karnaugh maps:

(a)

AB

CD	00	01	11	10
00	0	0	F	0
01	X	E	E+F	E
11	1	EF	0	$\bar{F}$
10	0	0	0	0

(b)

AB

CD	00	01	11	10
00	$\bar{E}$	1	$\bar{E}$	xE
01	xE	$xE+\bar{E}$	$x\bar{E}$	0
11	0	E	x	1
10	$xE+\bar{E}$	$E+ x\bar{E}$	0	0

F = _____   F = _____

17. (4 pts) Draw the output signal, Q for the J-K flip-flop below given the input signals J, K and Clk. Assume all signals are active high.
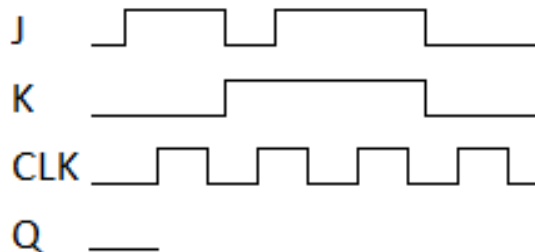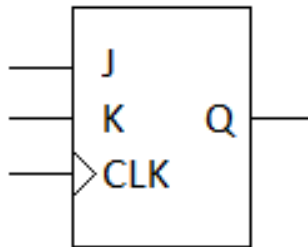
18. (8 pts) A shaft encoder generates a 2-bit gray code on signals A and B. Design an encoder circuit to convert this code to binary (Y_1Y_0) as shown in the truth table below. Assume all inputs and outputs are active high. You may use inverters, gates and/or multiplexors to perform this function. Show your schematic. (Hint: it may help to re-order the truth table so A and B are in binary order.)

A	B	Y_1	Y_0
0	1	0	0
1	1	0	1
1	0	1	0
0	0	1	1

19. (4 pts) One way to model the circuit in problem 18 starts with the entity declaration shown below. Write the architecture part, using just one conditional assignment statement in the body.

```
entitiy gray_conv is
    port(A, B: in std_logic; Y: out std_logic_vector(1 downto 0));
end gray_conv;
```

20. (8 pts) <u>Without</u> using arrays for test vectors, write a VHDL test bench that TESTS (not merely provides stimulus to) the model you created in problem 19.

21. (4 pts) The following VHDL process might be used in a test bench for the model in problem 19:

```
process
    variable vect: std_logic_vector(3 downto 0);
begin
    for i in 1 to 4 loop
        vect := test_vect(i);
        A <= vect(3); B <= vect(2);
        wait for 10ns;
        assert Y = vect(1 downto 0) report "wrong, wrong, so wrong!";
    end loop;
    wait;
end process;
```

Show how to declare **test_vect**. (Hint, you will need to declare its type first).

22. (4 pts) A certain circuit uses registers with $t_S = 3$ns, $t_H = 1$ns, $t_{P,CLK-Q} = 2.5$ns. What is the maximum allowable propagation delay through the combinational logic if the circuit is to operate with a 100MHz clock frequency?

_____ ns

23. (4 pts) Show how to create an SR latch from two NAND gates and use it to debounce the "double throw" switch shown below. (It is not necessary to show resistor values.)

S1
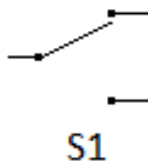
24. (15 pts) Name the device modeled by the VHDL code below. For flip-flops and counters, also state whether or not there is a clock enable and/or a reset, and if there is a reset, state whether it is synchronous or asynchronous:

a) **Y <= I0 when S = "00" else I1 when S = "01" else I2 when S = "10" else I3;**

device is:_____

b) **Y <= A when E = '1' else 'Z';**

device is:_____

c) **process (clk)**
   begin
       if rising_edge(clk) then
           if reset = '1' then
               Q <= '0';
           else
               Q <= D;
           end if;
       end if;
   end process;

device is:_____

d) **process (clk, reset)**
   begin
       if reset = '1' then
           Qi <= "0000";
       elsif rising_edge(clk) then
           if CE = '1' then
               Qi <= Qi + 1;
           end if;
       end if;
   end process;
   Q <= Qi;

device is:_____

e) **process (D, G)**
   begin
       if G = '1' then
           Q <= D;
       end if;
   end process;

device is:_____

Extra credit (3 pts) Solve problem 18 using only an encoder and a decoder.